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Physically Responsive Field-Effect Transistors with Giant Electromechanical Coupling Induced by Nanocomposite Gate Dielectrics

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ABSTRACT Physically responsive field-effect transistors (physi-FETs) that are sensitive to physical stimuli have been studied for decades. The important issue for separating the responses of sensing materials from interference by other subcomponents in a FET transducer under global physical stimuli has not been completely resolved. In addition, challenges remain with regard to the design and employment of smart materials for flexible physi-FETs with a large electro-physical coupling effect. In this article, we propose the direct integration of nanocomposite (NC) gate dielectrics of barium titanate (BT) nanoparticles (NPs) and highly crystalline poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) into flexible organic FETs to achieve a large electro-physical coupling effect. Additionally, a new alternating current biasing method is proposed for precise extraction and quantification of tiny variations in the remnant polarization of NCs caused by mechanical stimuli. An investigation of physi-FETs under static mechanical stimuli revealed the first ever reported giant, positive piezoelectric coefficients of d_{33} up to 960 pC/N in the NCs. The large coefficients are presumably due to the significant contributions of the intrinsic positive piezoelectricity of the BT NPs and P(VDF-TrFE) crystallites.

KEYWORDS: FETs · sensor · piezoelectric · P(VDF-TrFE) · nanocomposites

With the recent advances in flexible and stretchable electronics, the development of physically responsive field-effect transistors (physi-FETs) that are easily integrated into transformable substrates may enable ubiquitous physical sensing devices in electronic gadgets, allowing for the introduction of new functions. Flexible physi-FETs have been demonstrated to be responsive to mechanical strain,[1−7] electromagnetic coupling,[8] optical irradiation,[9,10] and thermal stimuli.[1,7,11,12] However, physical stimuli typically induce sensing signals from the entire physi-FET device under global influences that also cause changes in such FET transducer parameters as channel mobility, contact resistance, and dielectric capacitance. These changes prevent proper interpretations of the responses of sensing materials in physi-FETs. In an effort to isolate the response signals of sensing materials from interference by subcomponents in FET transducers, extended gate structures with isolated stimuli have recently been used in physi-FETs.[4,9,7,12] However, such approaches are limited to prototype research as isolated stimuli are rarely present in real-life applications, especially as device size decreases. Structural complexity, signal-to-noise ratio, and the power consumption of the entire device may also increase due to the need for additional interconnects.

Another challenge involves the use of smart materials with a large electro-physical coupling effect in highly responsive, flexible physi-FETs. In order to enhance electromechanical coupling, 0−3 nanocomposites (NCs) prepared using a hot-press process have received much attention.[4,7] In the hot-press process, piezoelectric nanoparticles (NPs) are embedded in an amorphous piezoelectric polymer. Materials prepared by this method have been extensively studied as they allow for a balance between the flexibility of the polymer matrix and the high functionality of inorganic NPs. However, the reported values for the d_{33} piezoelectric coefficients of 0−3 NCs have thus far been undesirably low despite the large d_{33} values of ceramic NPs.[13−16] Such low d_{33} values are due to the surrounding amorphous polymer that reduces the stress experienced by the NPs, which constrains the contribution of the NPs to the total d_{33}.

In this work, we theoretically and experimentally demonstrated that the direct integration of smart materials into flexible organic FETs (OFETs) as gate dielectrics led to physi-FETs with a simple device structure and allowed for a precise investigation of

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functional materials. Using static stimulations to investigate NCs of *highly crystalline* poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) and barium titanate (BT) NPs, we achieved giant, positive d_{33} values in the range of 120 to 960 pC N^{-1} depending on the fraction of BT NPs. When compared to published values of −10 to −40 pC N^{-1} for 0−3 NCs,[13] the d_{33} values obtained in this work are of opposite sign and 1 to 2 orders of magnitude greater. Such a difference is presumably due to the intrinsic positive piezoelectricity of anisotropic P(VDF-TrFE) crystallites and BT NPs. In previous works, the contributions of these two components in conventional 0−3 NCs were significantly smaller due to the viscoelasticity of amorphous P(VDF-TrFE).

RESULTS AND DISCUSSION

Electrical Characterization of Physi-FETs with Polarized Gate Dielectrics. Figure 1a shows the output characteristics of an as-fabricated highly crystalline NC device with 30 wt % BT NPs annealed at 140 °C (see Methods section). The BT NP/P(VDF-TrFE) nanocomposite gate dielectric layer did not initially possess a remnant polarization, P_r, as it was prepared by a solution process. As a result, the layer behaved like a normal gate dielectric material with typical output characteristics and saturation of the drain current (I_D) in the regions of low gate bias (V_G) and high drain bias (V_D). In order to induce piezoelectricity in the nanocomposite layer, a poling process is required so that P_r can be generated inside the BT/P(VDF-TrFE) nanocomposite layers. Figure 1b shows a schematic of the on-chip poling process[11] in which the source and drain electrodes were grounded while the gate electrode was connected to a negative bias. The accumulated conducting semiconductor layer and gate electrode served as poling electrodes that produced a uniform poling electric field across the gate dielectric layer. In the poling process, the applied poling electric field was 133 MV m^{-1} for the grounded source and drain electrodes, a V_G of −80 V, and a 600 nm thick gate dielectric. The output characteristics of the poled device at the same conditions measured for Figure 1a are shown in Figure 1c. All of the I_D−V_D curves eventually became linear, even in low V_G and high V_D regions where saturation of I_D should occur. Furthermore, the range of I_D in the poled device increased 3-fold, from 3 to 9 μA. The P_r induced inside the gate dielectric layer, which served as an additional high gate bias, can be used to explain these phenomena. An analytical investigation of these phenomena was conducted in our previous work,[11] in which the following equations for polarized gate dielectric OFETs were proposed:

$$P_r = \varepsilon_0 \varepsilon_r \frac{V_0}{d} \qquad (1)$$

$$I_D = \mu C \frac{W}{L}\left(\frac{1}{2}V_D{}^2 - (V_G + V_0)V_D\right) \qquad (2)$$

where V_0 is the equivalent external gate bias of P_r, μ is the effective channel mobility, C is the capacitance of the gate dielectric layer, and W and L are the width and length of the channel, respectively.

The dipole states of the BT NPs and P(VDF-TrFE) crystallites in the poled device can be confirmed by a depolarization process. The gate current (I_G) was recorded, while an electric field opposite the poling field was applied by sweeping V_G from 0 to 70 V and maintaining the V_D at −5 V. The results of this depolarizing process are shown in Figure 1d. Two clear I_G peaks, marked #1 and #2, were observed at V_G values of 35 and 50 V, respectively. These two peaks were attributed to the dipole switchings of P(VDF-TrFE) crystallites and BT NPs, which produced depolarizing currents in I_G. The equivalent electric fields of peaks #1 and #2 were 58.3 and 83.3 MV m^{-1}, respectively. Such results are in good agreement with the obtained coercive electric fields of P(VDF-TrFE)[17,18] and BT NPs[19,20] based on the local field effect experienced by NPs in a polymer matrix.[13,15,16] As a result, both BT NPs and the crystalline phase of P(VDF-TrFE) were successfully poled using the proposed on-chip poling process.

Separating Interferences in the Response Signals of Physi-FETs Due to the Gate Bias Method. The working principle of physi-FETs based on the direct piezoelectric effect is the conversion of external mechanical strains or stresses into changes in P_r or V_0. Such changes in turn modulate the read-out current I_D according to eqs 1 and 2. Figure 2a shows typical I_D responses of a poled 30 wt % NC device annealed at 140 °C and measured at $V_G = 0$ V and $V_D = -5$ V at different pressures. It should be noted that other electrical parameters such as the effective channel mobility and gate dielectric capacitance typically respond to global mechanical stimuli (see Figure 2b) and interfere with the modulated I_D. Thus, a clear separation between the response of the direct piezoelectricity and other electrical parameters is essential for investigating and developing highly functional materials for physi-FETs.

In order to address the above issue, we propose a simple and novel technique, called the alternative current (ac) gate bias method that generally eliminates unwanted electrical interferences. A sinusoidal potential with known frequency, a relatively small amplitude compared to V_0, and no DC background were applied to the gate electrode. Through the application of several simple mathematical transforms (see equations in Supporting Information), the following equation was developed based on eq 2:

$$I_D = -\mu C \frac{W}{L} V_{G0} V_D \sin(2\pi f t + \varphi) - \mu C \frac{W}{L} V_0 V_D \qquad (3)$$

where V_{G0} and f are the amplitude and frequency of the applied gate bias, respectively. The first term in eq 3 corresponds to the contribution of an intentionally

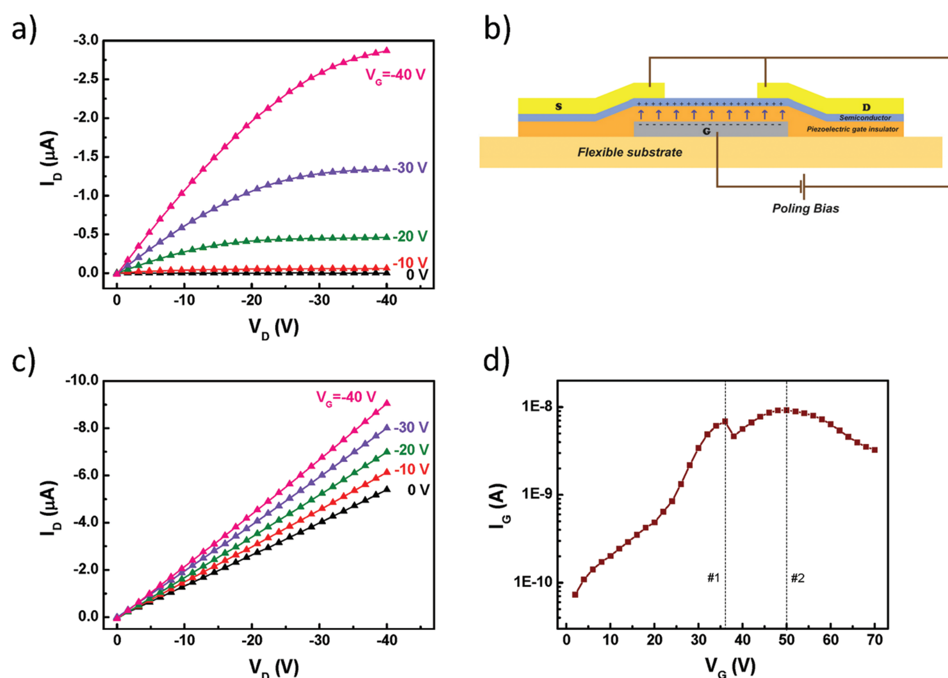

Figure 1. Fundamental electrical characteristics of physi-FETs with a NC gate dielectric of 30 wt % BT NPs and highly crystalline P(VDF-TrFE). (a) Output characteristics of as-fabricated physi-FETs; their characteristics are similar to those of conventional FETs. (b) Schematic of the on-chip poling process for physi-FETs. The accumulated semiconductor layer and gate electrode serve as poling electrodes and produce a uniform poling electric field across the piezoelectric gate insulator layer. (c) Output characteristics of the poled physi-FETs; I_D becomes linear rather than saturated in low V_G−high V_D regions, implying that a high P_r was produced in the piezoelectric gate insulator layer. (d) Dipole switching of P(VDF-TrFE) crystallites and BT NPs in poled physi-FETs. Two I_G peaks are observed when applying an electric field opposite to that of the poling electric field, indicating that the P(VDF-TrFE) crystallites and BT NPs were successfully poled by the on-chip poling process.

applied sinusoidal gate bias to I_D, while the second term is the contribution of V_0 or P_r. Although μ, C, W, L, V_D, V_{G0}, and V_0 can affect the amplitude, the value of V_0 can be accurately interpreted from the ratio of the amplitude and mean values of I_D ($I_D^{amp} = -\mu C(W/L)V_{G0}V_D$ and $I_D^{mean} = -\mu C(W/L)V_0V_D$), regardless of the interferences from other parameters:

$$V_0 = V_{G0}\frac{I_D^{mean}}{I_D^{amp}} \quad (4)$$

Figure 2c shows the time dependence of I_D *versus* applied pressure for a poled, 30 wt % highly crystalline NC device using the ac gate bias method with $V_D = -5$ V and $V_G = 5\sin(2\pi 0.5t + \varphi)$. Parameters V_D, V_{G0}, and f were −5 V, 5 V, and 0.5 Hz, respectively. In region (ii), both I_D^{amp} and I_D^{mean} increased as soon as pressure was applied. However, I_D appeared to be unstable with no generation of regular sinusoidal shapes. When the applied pressure reached 0.5 N/mm^2 and was maintained in region (iii), I_D^{amp} and I_D^{mean} gradually decreased. Then, I_D^{mean} in region (iv) continued to decrease, while I_D^{amp} was unchanged. Finally, I_D^{amp} and I_D^{mean} became stationary in region (v).

Since the change in C (0.2%) was negligible at an applied pressure of 0.5 N/mm^2 when compared to the change in μ (5%) (see Figure 2b), changes in I_D^{amp} in Figure 2c were ascribed mainly to interference by changes in μ according to eq 3. When suddenly exposed to compressed N_2 gas, a pentacent layer may experience mechanical non-equilibrium that results in a sudden rise and instability in μ or I_D^{amp} in region (ii). Relaxation may then occur which serves to reduce μ as I_D^{amp} decreases in region (iii). After relaxation, μ becomes stationary as I_D^{amp} is maintained in regions (iv) and (v). The increase in μ under pressure[21,22] contributed to a 0.119 μA increase in I_D^{amp} in region (iii) compared to an increase of 0.116 μA in region (i). Similar observations were also made for the normal FET structure with a nonpolar gate dielectric of poly(vinyl phenol) (Supporting Information Figure S1). The effects of pressure on μ in regions (vi), (vii), (viii), and (ix) are analogous to those described in the preceding discussion.

Since μ was stationary in region (iv), the slow decrease and increase in I_D^{mean} (inset of Figure 3c) was ascribed to changes in V_0 according to eq 3. After tens of seconds, V_0 in region (v) became stable. A similar behavior of V_0 in regions (iv), (v), (viii), and (ix) indicated that the transients were time-limited and unavoidable. Thus, stable values of V_0, and thus P_r, can be precisely estimated from equilibrium in regions (i), (v), and (ix) in Figure 2c according to eqs 1 and 4.

Value of d_{33} of Highly Crystalline BT/P(VDF-TrFE) NCs. The test results for the reliability of the P_r measurements, as interpreted using the proposed ac gate bias method, are shown in Figure 3a. A 40 wt % highly crystalline NC device annealed at 140 °C was subjected to a repeating

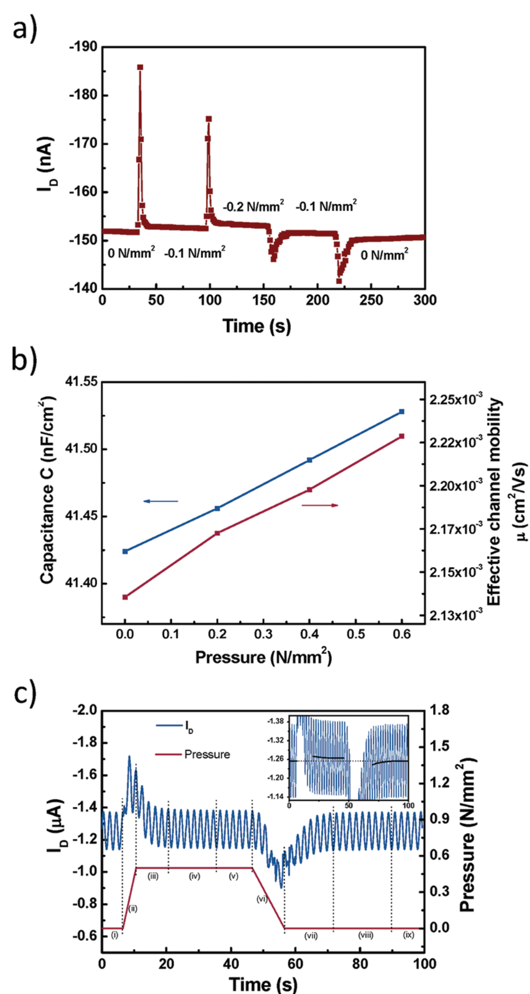

Figure 2. Interferences by subcomponents in a 30 wt % NC physi-FET and the proposed ac gate bias method for precisely separating responses of the piezoelectric gate insulator layer from interferences. (a) Modulated read-out I_D of the device at different applied pressures. Responses of the piezoelectric gate dielectric layer cannot be distinguished from the modulated I_D. (b) Pressure dependence of the gate dielectric capacitance and mobility of the pentacene layer. The changes in the physi-FET properties produced interferences in the read-out I_D. (c) Proposed ac gate bias method for precisely interpreting responses of the piezoelectric gate insulator. By taking the ratio of the amplitude to the mean value of I_D at the equilibrium regions, such as regions (i), (iii), and (v), the responses of the piezoelectric gate dielectric layer to the global pressure can be accurately extracted.

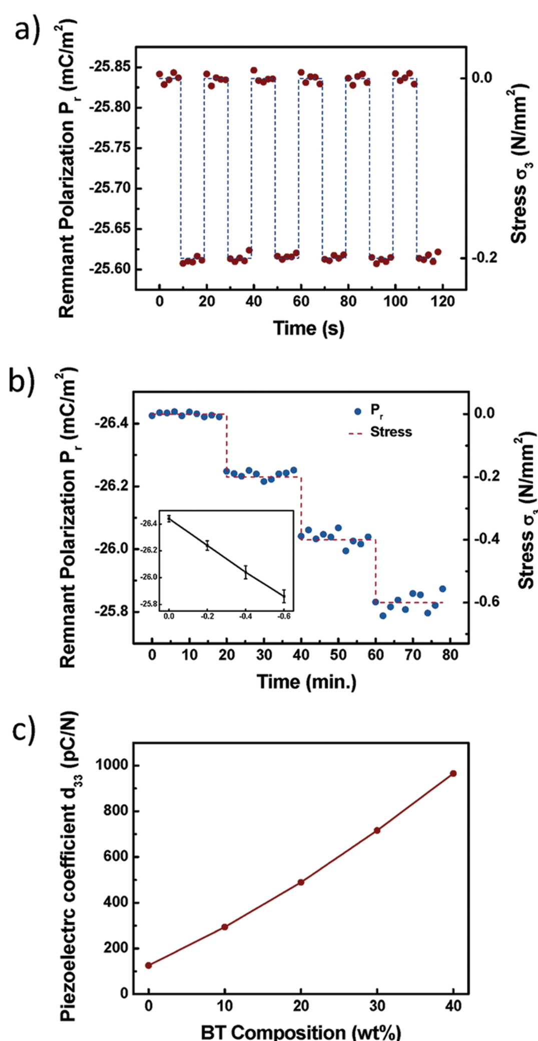

Figure 3. Measurement of reliability using the ac gate bias method and the piezoelectric coefficients (d_{33}) of NCs of BT NPs and highly crystalline P(VDF-TrFE). (a) Ac gate bias method reveals a stable and reliably interpreted P_r. (b) Changes in P_r at different applied stresses σ_3. The value of d_{33} can be determined from the slope of the P_r–σ_3 correlation line. (c) Interpreted d_{33} values of NCs of BT NPs and highly crystalline P(VDF-TrFE) with varied compositions of BT NPs; the values are opposite in sign and enhanced by 1–2 orders of magnitude when compared to conventional 0–3 NCs.

stress σ_3 of -0.2 N mm^{-2} over 2 h. Each value of P_r was obtained in equilibrium regions at 2 min intervals. Stable and repeatable P_r values in Figure 3a indicated that our proposed ac gate bias method for physi-FETs with a piezoelectric gate insulator was reliable. The changes in P_r at different σ_3 values are shown in Figure 3b. P_r values at the same stress were similar; however, as more pressure was applied, more deviation in the interpreted P_r values was observed. This is due to the instability in the semiconductor conductivity at high pressure, which prevents the precise determination of I_D^{amp}. On the basis of the definition of the piezoelectric coefficient, $d_{33} = \Delta|P_r|/\Delta\sigma_3$, the slope of the linear P_r–σ_3 correlation line (inset in Figure 3b) can be used to obtain an accurate estimate of d_{33} (960 pC N^{-1}).

The d_{33} values of highly crystalline BT/P(VDF-TrFE) NCs annealed at 140 °C with different amounts of BT NPs are shown in Figure 3c. The values were calculated from the linear P_r–σ_3 curves for physi-FETs (see an example of a 40 wt % NC physi-FET in Figure 3b). The obtained d_{33} values were in the range of 120–960 pC N^{-1}. Such values are significantly different in both sign and magnitude from previously reported values of 0–3 NCs, which were in the range of -10 to -40 pC/N.[13] Such discrepancy may be due to the differences in crystallinity of the examined samples and in the frequency of the mechanical stimuli during measurement.

Examining the Role of P(VDF-TrFE) Crystallinity in the Total d_{33} Coefficients. It should be noted that the conventional 0−3 NCs analyzed in previous studies[13−16] were fabricated *via* the hot-press process, which yielded a very large amount of amorphous P(VDF-TrFE) phase. To gain a better understanding of the effect of P(VDF-TrFE) crystallinity on the total d_{33} in NCs, we investigated the fundamental two-phase system (amorphous and crystalline phases) for semicrystalline P(VDF-TrFE) copolymers without BT NPs. The interpreted d_{33} values of four P(VDF-TrFE) devices with P(VDF-TrFE) gate dielectric layers annealed at temperatures from 80 to 140 °C are shown in Figure 4a. These annealing conditions would produce P(VDF-TrFE) thin films with different fractions of amorphous and crystalline phases. The XRD data (inset of Figure 4a) clearly showed that samples annealed at a higher temperature possessed a higher degree of crystallinity. In Figure 4a, the values of d_{33} in the P(VDF-TrFE) devices varied from −60 to 120 pC N^{-1} for annealing temperatures of 80 to 140 °C. The tendency of d_{33} to shift in the positive direction for higher crystalline P(VDF-TrFE) thin films, as well as the crossover above the zero point in Figure 4a, implied that the amorphous and crystalline P(VDF-TrFE) phases have opposite effects (negative and positive piezoelectricity, respectively) on the total d_{33} values. This observation is consistent with the well-known explanation that the deformation absorption of the amorphous matrix results in negative d_{33} coefficients for PVDF and P(VDF-TrFE) thin films.[23−25] In another study that involved the use of piezoresponse force microscopy, single-crystal-like P(VDF-TrFE) thin films possessed a positive d_{33}, which also corroborates our observations.[26]

In order to explain the trend illustrated in Figure 4a, the spatial conformations of thin films should be considered. A schematic of a P(VDF-TrFE) thin film with a low degree of crystallinity is shown in Figure 4b. The surrounding amorphous matrix absorbed more strain and reduced the stress experienced by small-size crystallites under pressure. This phenomenon was reported in previous theoretical works, where rigid bodies embedded in a soft polymer matrix experienced reduced stresses.[27,28] Therefore, the contribution of the positive piezoelectricity of P(VDF-TrFE) crystallites to the total d_{33} was limited in low crystallinity P(VDF-TrFE). However, when the P(VDF-TrFE) crystalline phase is dominant (Figure 4c), the thin layer of the amorphous phase cannot prevent crystallite compression, and thus, the significant contribution of their positive intrinsic piezoelectricity to the total d_{33} coefficient is revealed. Depending on the amount of crystallinity in the films, the contributions of the two opposing effects determine the total d_{33} values.

The d_{33} coefficients of low crystallinity NCs annealed at 80 °C with the same composition of BT NPs as that of the highly crystalline NCs in Figure 3c are shown in Figure 4d. The small d_{33} values in Figure 4d compared to those in Figure 3c confirm the minor

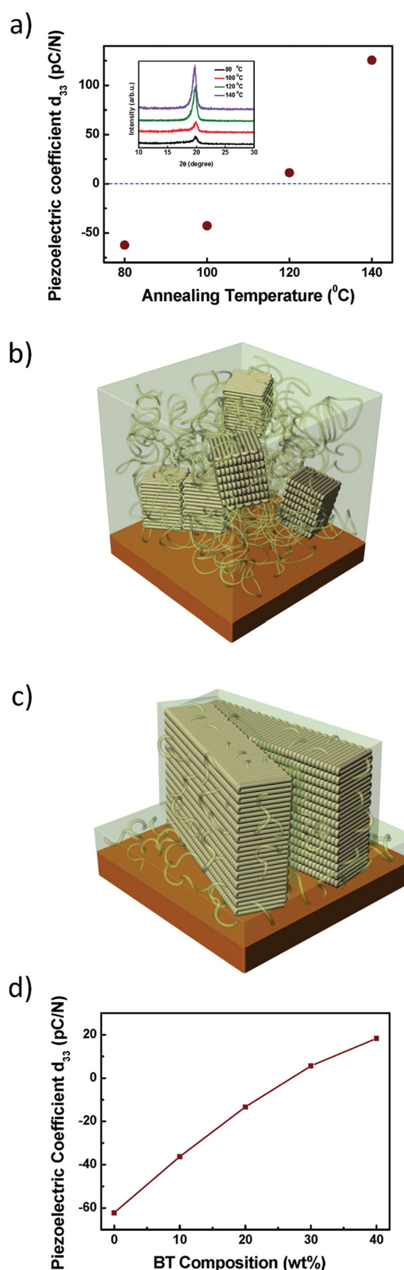

Figure 4. Role of highly crystalline P(VDF-TrFE) in the total d_{33} piezoelectric coefficients. (a) Interpreted d_{33} of P(VDF-TrFE) thin films at different annealing temperatures. A higher annealing temperature yields a higher crystallinity (XRD data in the inset). The crossover at the zero point implies opposite effects of the P(VDF-TrFE) amorphous and crystalline phases (negative and positive piezoelectricity, respectively). (b) Schematic of a low crystallinity P(VDF-TrFE) thin film. The surrounding amorphous polymer absorbs most of the strain and prevents embedded crystallites from experiencing stress, thus yielding a negative piezoelectricity. (c) Schematic of a highly crystalline P(VDF-TrFE) thin film. Large crystallites covered by a thin layer of amorphous polymer experienced an applied stress and contributed their positive intrinsic piezoelectricity to the total d_{33}. (d) In low crystallinity 40 wt % NCs annealed at 80 °C, the BT NPs have minor contributions (as confirmed by the small d_{33} values) due to the large quantity of the surrounding amorphous P(VDF-TrFE) phase.

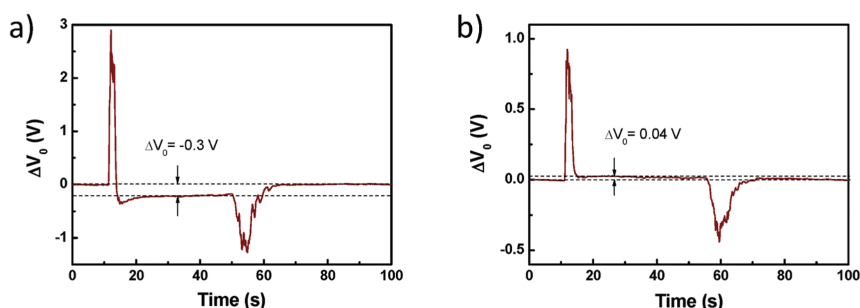

Figure 5. Result validation from the ac gate bias method by direct measurement. (a) Changes in the V_0 of highly crystalline 40 wt % NCs. The V_0 decreases by 0.3 V at an applied stress σ_3 of -0.2 N/mm^2, resulting in a d_{33} value of 800 pC/N. This value is comparable to the 960 pC/N value measured in the physi-FET structure using the ac gate bias method. (b) Changes in the V_0 of low crystalline P(VDF-TrFE). The increase in V_0 by 0.04 V at an applied stress of -0.2 N/mm^2 resulted in a d_{33} value of -54.6 pC/N, which is comparable to -62.2 pC/N measured in a physi-FET structure using the ac gate bias method.

contributions from BT NPs and P(VDF-TrFE) crystallites when they are embedded in an amorphous P(VDF-TrFE) matrix.

Result Validation of Physi-FETs by Direct Measurement Method. We performed direct measurements of piezoelectric coefficients using a metal/insulator/metal (MIM) structure to validate the proposed ac gate bias method for physi-FETs. After poling, the remnant polarization of NC thin films in the MIM structure was compensated by free charges at the metal electrodes. Thus, there was a screening effect that induces 0 V across the two electrodes. As such, direct measurement of the voltage between the electrodes at different pressures revealed only changes in V_0 (ΔV_0). The changes in V_0 for a poled highly crystalline, 40 wt % NC thin film when a stress σ_3 of -0.2 N/mm^2 was introduced and released are shown in Figure 5a. Similar to the case of pentacene (Figure 2), a sudden exposure to pressure by compressed N_2 gas also caused mechanical non-equilibrium followed by relaxation in the BT/P(VDF-TrFE) thin film. For a steady-state scenario, the measured ΔV_0 was -0.3 V. According to Supporting Information eqs 11 and 12, the change in the surface charge density of the investigated NC thin film was $\Delta Q_s = C\Delta V_0 = -16.02 \times 10^{-5}$ C/m^2, with a measured capacitance C of 53.4 nF/cm^2. From Supporting Information eq 13, the d_{33} coefficient was calculated as $d_{33} = \Delta Q_s/\Delta\sigma_3 = 800$ pC/N. This value is comparable to the 960 pC/N (Figure 2c) value measured in the physi-FET structure. Changes in the V_0 of low crystalline P(VDF-TrFE) in the MIM structure are shown in Figure 5b. With a measured capacitance of 27.3 nF/cm^2, the 0.04 V increase in V_0 at an applied stress of -0.2 N/mm^2 resulted in a d_{33} value of -54.6 pC/N. This value is comparable to the -62.2 pC/N value obtained from the physi-FET structure.

The effect of contact resistance, R_c, on I_D modulation under pressure due to changes in P_r was also examined. The total resistances, R_{total}, of highly crystalline devices at different channel lengths, L, were measured (Supporting Information S2). R_c values were determined by half of the extrapolated intercepts of the $R_{total}-L$ line. The experimental results showed that the contribution of R_c to R_{total} was less than 2%. Moreover, variations in R_c at different applied pressure were virtually undetectable (Supporting Information Table S2).

The static stimulation investigation may be another reason for the giant, positive d_{33} values in highly crystalline NCs. In previous works,[13−16] where characterizations were performed in the high frequency regime of mechanical stimuli (~kHz), stress propagation and creep deformation occurred simultaneously in the amorphous P(VDF-TrFE) due to viscoelasticity. The direct observations obtained by monitoring the change in V_0 for a MIM structure showed that these transition processes occur for up to several seconds (Figure 5a,b). Thus, the applied stress in such a short period may not be fully transferred to the rigid BT NPs and P(VDF-TrFE) crystallites, resulting in minor contributions of their intrinsic piezoelectricities to the total d_{33}. In contrast, the P_r of our highly crystalline NCs was investigated after the applied stresses were fully transferred to the BT NPs and P(VDF-TrFE) crystallites, as in regions (i), (iii), and (v) in Figure 2c. The negative shift d_{33} value at higher stimuli frequencies was observed by monitoring transient behavior of the I_D at different stimulation periods of applied pressure (Supporting Information Figure S3).

From the d_{33} values of highly crystalline NCs, the d_{33} of P(VDF-TrFE) crystallites and BT NPs can be roughly estimated as 120 and 2000 pC N^{-1}, respectively, using a simple linear superposition model, $d_{33}^{total} = (1 - w)d_{33}^{P(VDF-TrFE)} + wd_{33}^{BTNPs}$, where w is the weight fraction of the BT NPs. It is notable that the extracted value of 120 pC N^{-1} for P(VDF-TrFE) crystallites was less than the ~250 pC N^{-1} value obtained for a single-crystal-like thin film.[26] The smaller d_{33} value extracted from the P(VDF-TrFE) crystallites may be due to a small amount of amorphous phase in our sample. Although the amount of amorphous phase in the highly crystalline P(VDF-TrFE) and NCs was small, it would partially negatively contribute to the total d_{33}. The extremely high value of 2000 pC N^{-1} for the BT NPs is consistent

with predictions of enhanced in piezoelectricity by flexoelectricity when the domain size of the BT is reduced to tens of nanometers.[29−31] Thus, the intrinsic positive piezoelectricity of BT NPs and highly crystalline P(VDF-TrFE) primarily contributed to the total piezoelectricity and led to giant, positive d_{33} values of 960 pC N^{-1}.

CONCLUSIONS

We theoretically and experimentally demonstrated for the first time that the direct integration of smart materials into flexible OFETs allows for both the development of physi-FETs with a simple device structure and the capability to detect extremely small response signals with a high level of accuracy. The interference of other parameters such as the channel mobility and capacitance were effectively avoided using the proposed ac gate bias method. On the basis of the proposed method, apparent giant, positive d_{33} values for BT/P(VDF-TrFE) NCs under static conditions were measured in physi-FETs. Changes in sign and an increase in d_{33} magnitude by 1−2 orders were attributed to flexoelectricity, the high intrinsic piezoelectricity of anisotropic P(VDF-TrFE) crystallites, and the BT NPs. Compared to recent approaches, the direct integration of functional gate insulators can provide various advantages when embedding physi-FETs into transformable integrated circuits. Such advantages include the elimination of additional circuitry, the ability to embed submicrometer-sized physi-FETs, ease of arraying, lower power consumption, and various choices of smart materials. Supporting Information Figures S3 and S4 demonstrate the capability of extending our physi-FETs to sense responses to mechanical strain and IR irradiation.

METHODS

P(VDF-TrFE) (65 mol % of VDF) was purchased from Piezotech S.A. BT NPs with an average diameter of 50 nm and the coupling agent 3-aminopropyltriethoxy silane (APTES) were purchased from Sigma Aldrich. The BT NPs were first ball-milled for 2 h to separate aggregated NPs. After milling, the BT NPs were dispersed in an APTES/ethanol solution with a pH of 4−4.5 (adjusted by HCl) for 1 h. The mixture of BT NPs and APTES/ethanol was filtered and washed in ethanol to remove residual APTES. The treated BT NPs were then cured at 110 °C for 5 min on a hot plate and mixed with *N*,*N*-dimethylformamide (DMF). Centrifugation was performed to produce a solvent−particle mixture with small BT NPs. P(VDF-TrFE) and DMF were added to produce solutions of 1 g of P(VDF-TrFE) in 10 mL of DMF with a predefined wt % of BT NPs with respect to P(VDF-TrFE). An inverted-staggered bottom-contact OFET structure with Ni as gate electrode, pentacene as organic semiconductor, and Au as source/drain electrodes was used. Highly crystalline BT/P(VDF-TrFE) NC gate dielectric layers were obtained by annealing at 140 °C for 2 h. The physi-FET device fabrication process was previously described in detail.[11] The preparation procedures for low crystallinity P(VDF-TrFE) and NC physi-FETs are similar to the process described above, except that the gate dielectric layers were crystallized by annealing the samples at the specified temperature for 1 h.

The output and transfer characteristics of the devices were measured with an HP 1415B semiconductor parameter analyzer. The channel dimensions of the characterized devices were 40 μm in length and 800 μm in width. Pressurization measurements were performed in a closed metallic chamber with the aid of compressed N_2. Unless otherwise stated, the ac gate bias method was used by applying a sinusoidal voltage with an amplitude of 2 V and a frequency of 0.5 Hz to the gate electrode while V_D was maintained at −5 V. The capacitance of the P(VDF-TrFE) in a metal−insulator−metal structure was measured with an Agilent E4980A precision LCR meter.

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Supporting Information Available: Additional equations and figures. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

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